CLAIMS

1. An information processing apparatus comprising:

receiving means for receiving a stream constructed by packets of a predetermined format;

extracting means for extracting the packets which are recorded to a recording apparatus from the packets constructing said stream received by said receiving means;

memory means for storing said packets extracted by said extracting means;

a command buffer for forming a command for instructing a DMA transfer; and

transfer means for DMA-transferring said packets to said recording apparatus by using the packets as a block of a predetermined data amount in accordance with said command formed in said command buffer.

2. An information processing apparatus according to claim 1, wherein said command to instruct said DMA transfer is formed in the case where the data amount of said packets stored by said memory means reaches a predetermined capacity.

3. An information processing apparatus according to claim 1, wherein said memory means is constructed by an input FIFO and an output FIFO.

4. An information processing apparatus according to claim 3, wherein said command to instruct said DMA transfer is formed in the case where the data amount of said packets stored in said input FIFO is equal to or larger than a predetermined capacity.

5. An information processing apparatus according to claim 3, wherein said command to instruct said DMA transfer is formed in the case where the data amount of said packets stored in said output FIFO is equal to or smaller than the predetermined capacity.

6. An information processing apparatus according to claim 1, further comprising adding means for adding address information including at least one of an address in said recording apparatus in which a just-previous block has been recorded, an address in said recording apparatus in which a current block is recorded, and an address in said recording apparatus in which a just-subsequent block is recorded to said packets.

7. An information processing apparatus according to claim 1, wherein said recording apparatus is a hard disk drive built in said information processing apparatus.

8. An information processing apparatus comprising:

receiving means for receiving a stream constructed by packets of a predetermined format;

extracting means for extracting the packets which are recorded to a recording apparatus from the packets constructing said stream received by said receiving means;

memory means for storing said packets extracted by said extracting means;

a command buffer for setting address information for DMA transfer; and

adding means for adding said set address

information every predetermined data amount (block) of the packets read out from said memory means.

9. An information processing apparatus according to claim 8, wherein said adding means adds the address information including at least one of an address in said recording apparatus in which a just-previous block has been recorded, an address in said recording apparatus in which a current block is recorded, and an address in said recording apparatus in which a just-subsequent block is recorded to said block.

10. An information processing apparatus according to claim 8, further comprising updating means for updating said set address information for DMA transfer.

11. An information processing apparatus according to claim 10, wherein said updating means has an internal counter for automatically setting said address information.

12. An information processing apparatus according to claim 11, wherein as said address information, each time the DMA transfer of one block is finished, said internal counter is counted up and the address information of one block is set.

13. An information processing apparatus according to claim 10, wherein said updating means updates said address information for DMA transfer when the data amount of said packets stored by said memory means reaches a predetermined capacity.

14. An information processing apparatus according to

claim 8, wherein said memory means is constructed by an input FIFO and an output FIFO.

15. An information processing apparatus according to claim 14, further comprising updating means for updating said set address information for DMA transfer.

16. An information processing apparatus according to claim 15, wherein said updating means updates said address information for DMA transfer when the data amount of said packets stored in said input FIFO is equal to or larger than a predetermined capacity.

17. An information processing apparatus according to claim 15, wherein said updating means updates said address information for DMA transfer when the data amount of said packets stored in said output FIFO is equal to or smaller than a predetermined capacity.

18. An information processing apparatus according to claim 8, wherein said recording apparatus is a hard disk drive built in said information processing apparatus.

19. A digital broadcast receiving apparatus having a hard disk drive therein, comprising:

receiving means for receiving a stream constructed by packets of a predetermined format;

extracting means for extracting the packets which are recorded into said hard disk drive from the packets constructing said stream received by said receiving means;

memory means for storing said packets extracted by said extracting means;

a command buffer for forming a command for instructing a DMA transfer; and

transfer means for DMA-transferring said packets to said hard disk drive by using the packets as a block of a predetermined data amount in accordance with said command formed in said command buffer.

20. A digital broadcast receiving apparatus according to claim 19, wherein said command to instruct said DMA transfer is formed in the case where the data amount of said packets stored by said memory means reaches a predetermined capacity.

21. A digital broadcast receiving apparatus according to claim 19, wherein said memory means is constructed by an input FIFO and an output FIFO.

22. A digital broadcast receiving apparatus according to claim 21, wherein said command to instruct said DMA transfer is formed in the case where the data amount of said packets stored in said input FIFO is equal to or larger than a predetermined capacity.

23. A digital broadcast receiving apparatus according to claim 21, wherein said command to instruct said DMA transfer is formed in the case where the data amount of said packets stored in said output FIFO is equal to or smaller than a predetermined capacity.

24. (AMNDED)

A digital broadcast receiving apparatus according to claim 19, further comprising adding means for

adding address information including at least one of an address in said hard disk drive in which a just-previous block has been recorded, an address in said hard disk drive in which a current block is recorded, and an address in said hard disk drive in which a just-subsequent block is recorded to said packets.

25. (AMENDED)

A digital broadcast receiving apparatus having a hard disk drive therein, comprising:

receiving means for receiving a stream constructed by packets of a predetermined format;

extracting means for extracting the packets which are recorded into said hard disk drive from the packets constructing said stream received by said receiving means;

memory means for storing said packets extracted by said extracting means;

~~a command buffer for setting address information~~ for DMA transfer; and

adding means for adding said set address information every predetermined data amount (block) of the packets read out from said memory means.

26. (AMENDED)

A digital broadcast receiving apparatus, according to claim 25, wherein said adding means adds the address information including at least one of an address in said hard disk drive in which a just-previous block has been recorded, an address in said hard disk drive in which

a current block is recorded, and an address in said hard disk drive in which a just-subsequent block is recorded to said block.

27. (AMENDED)

A digital broadcast receiving apparatus, according to claim 25, further comprising updating means for updating said set address information for DMA transfer.

28. (AMNDED)

A digital broadcast receiving apparatus according to claim 27, wherein said updating means has an internal counter for automatically setting said address information.

29. (AMENDED)

A digital broadcast receiving apparatus according to claim 28, wherein as said address information, each time the DMA transfer of one block is finished, said internal counter is counted up and the address information of one block is set.

30. (AMENDED)

A digital broadcast receiving apparatus according to claim 27, wherein said updating means updates said address information for DMA transfer when the data amount of said packets stored by said memory means reaches a predetermined capacity.

31. (AMENDED)

A digital broadcast receiving apparatus according to claim 25, wherein said memory means is

constructed by an input FIFO and an output FIFO.

32. (AMENDED)

A digital broadcast receiving apparatus according to claim 31, further comprising updating means for updating said set address information for DMA transfer.

33. (AMENDED)

A digital broadcast receiving apparatus according to claim 32, wherein said updating means updates said address information for DMA transfer when the data amount of said packets stored in said input FIFO is equal to or larger than a predetermined capacity.

34. (AMENDED)

A digital broadcast receiving apparatus according to claim 32, wherein said updating means updates said address information for DMA transfer when the data amount of said packets stored in said output FIFO is equal to or smaller than a predetermined capacity.

35. (AMENDED)

An information processing method comprising:

a receiving step of receiving a stream constructed by packets of a predetermined format;

an extracting step of extracting the packets which are recorded to a recording apparatus from the packets constructing said stream received by said receiving step;

a storing step of storing said packets extracted by said extracting means;

a forming step of forming a command for instructing

a DMA transfer by a command buffer; and

a transfer step of DMA-transferring said packets to said recording apparatus by using the packets as a block of a predetermined data amount in accordance with said command formed in said forming step.

36. (AMENDED)

An information processing method comprising:

a receiving step of receiving a stream constructed by packets of a predetermined format;

an extracting step of extracting the packets which are recorded to a recording apparatus from the packets constructing said stream received by said receiving step;

a storing step of storing said packets extracted by said extracting step;

a setting step of setting address information for DMA transfer by a command buffer; and

an adding step of adding said set address information every predetermined data amount (block) of the packets read out from said memory means.

37. (AMENDED)

A recording medium in which a computer-readable program has been recorded, wherein said program comprises:

a receiving step of receiving a stream constructed by packets of a predetermined format;

an extracting step of extracting the packets which are recorded to a recording apparatus from the packets constructing said stream received by said receiving step;

a storing step of storing said packets extracted by said extracting means;

a forming step of forming a command for instructing a DMA transfer by a command buffer; and

a transfer step of DMA-transferring said packets to said recording apparatus by using the packets as a block of a predetermined data amount in accordance with said command formed in said forming step.

38. (AMENDED)

A recording medium in which a computer-readable program has been recorded, wherein said program comprises:

a receiving step of receiving a stream constructed by packets of a predetermined format;

an extracting step of extracting the packets which are recorded to a recording apparatus from the packets constructing said stream received by said receiving step;

a storing step of storing said packets extracted by said extracting step;

a setting step of setting address information for DMA transfer by a command buffer; and

an adding step of adding said set address information every predetermined data amount (block) of the packets read out from said memory means.

39. (DELETED)

40. (DELETED)